**SRI LANKA INSTITUTE OF ADVANCED TECHNOLOGICAL EDUCATION**

**-SLIATE-**

**COMPUTER ARCHITECTURE**

**5 YEARS PAST PAPERS**

SUBMITTED TO

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SUBMITTED BY

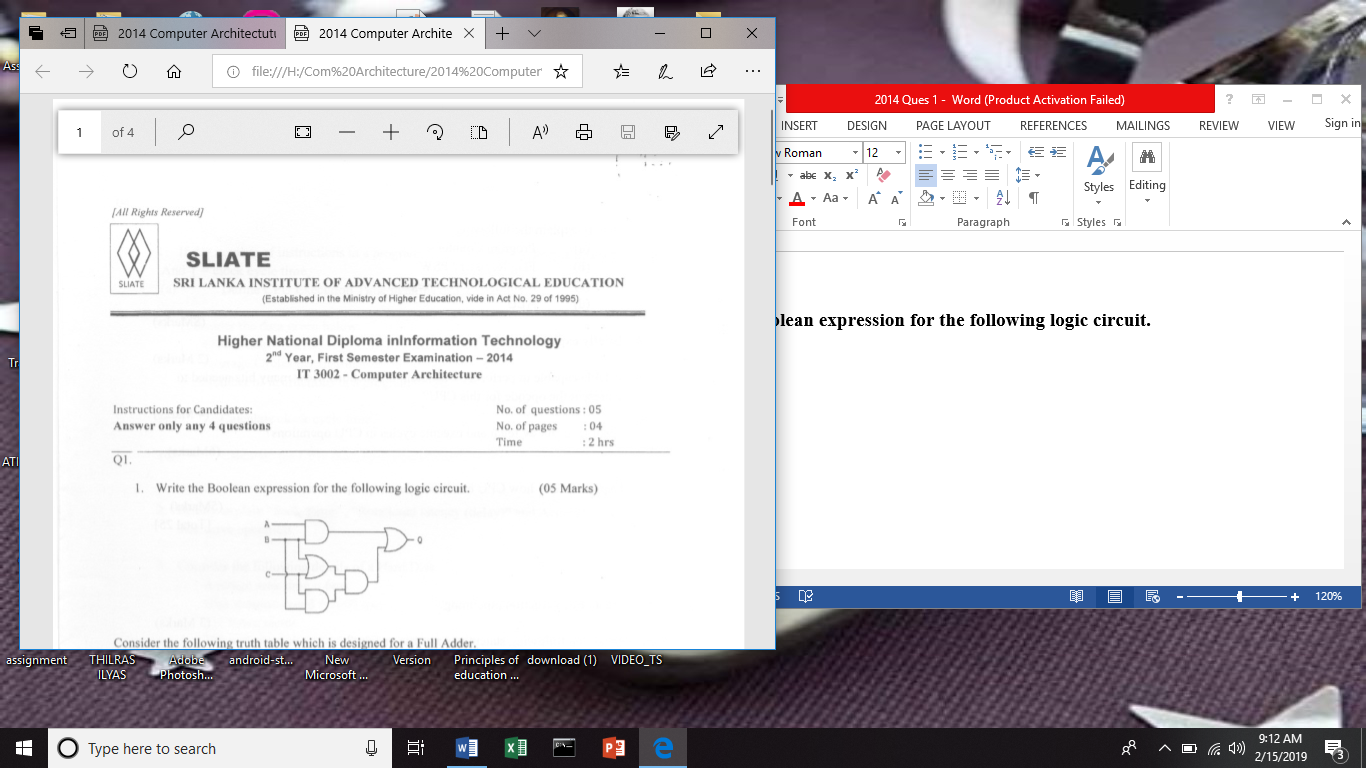
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**BAT/IT/2018/FT/030**

**2014**

**Q 01**

1. Write the Boolean expression for the following logic circuit.



* A.B+ ((B+C).(B.C))

Consider the following truth table which is designed for a full Adder

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| inputs | | | outputs | |
| x | y | Carry in | sum | Carry out |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

1. Drive logic equations for sum and carry out the above truth table?
2. Construct a logic circuit using XOR gates and basic gates for the full adder using the logic equations derived in above?
3. Simplify the following Boolean function F using K-map

F=ABC+A’B’C’+AB’C+ABC’

BC BC’ B’C’ B’C

|  |  |  |  |
| --- | --- | --- | --- |
| 1 | 1 | 0 | 1 |
| 0 | 0 | 1 | 0 |

**A**

F = AB+AC+A’B’C’

**A’**

**Q 02**

1. Briefly explain the following:
2. **Program Counter (PC)**

* A program counter is a register in a computer processor that contains the address (location) of the instruction being executed at the current time. After each instruction is fetched, the program counter points to the next instruction in the sequence.

1. **Flag Register / PSW**

* The FLAGS register is the status register in Intel ×86 microprocessors that contains the current state of the processor.

1. **Memory Address Register (MAR)**

* Memory Address Register specifies the address in memory of the data to be written from or read into the MBR.

1. **Arithmetic and Logical Unit (ALU)**

* Arithmetic Logic Unit is a digital circuit that performs integer arithmetic and logical operations. The ALU is a fundamental building block of the central processing unit of a computer.

1. Briefly explain Opcode?

* An opcode (abbreviated from operation code) is the portion of a machine language instruction that specifies the operation to be performed.

1. A CPU capable to perform 32 different instructions. How many bits needed to represent the opcode for this CPU?
2. What is meant by fetch and execute cycles in CPU operations?

* **Fetch**:

IR is examined

If indirect addressing, indirect cycle is performed

* Rightmost n bits of MBR (address part of instruction) transferred to MAR
* Control unit requests memory read
* Result (address of operand) moved to MBR
* **Execute:**

May take many forms, depends on instruction being executed

May include

* Memory read/write
* Input / Output
* Register transfers
* ALU operations

1. Explain briefly how CPU handles an interrupt operation?

* An interrupt handler, also known as an interrupt service routine or ISR, is a callback function in microcontroller firmware, an operating system or a device driver, whose execution is triggered by the reception of an interrupt. Interrupt handlers have a multitude of functions, which vary based on the reason the interrupt was generated and the speed at which the interrupt handler completes its task.

**Q 03**

1. What is mean by instruction pipelining?

* An instruction pipeline is a technique used in the design of computers to increase their instruction throughput. The basic instruction cycle is broken up into a series called a pipeline. Rather than processing each instruction, each instruction is split up into a sequence of steps so different steps can be executed concurrently and in parallel.

1. State weather the following statements are true or false?
2. Execution time of an instruction will be increased by Pipelining. (True/False)?

* True

1. Execution time of a program will be increased by Pipelining. (True/False)?

* False

1. We can increase the performance of a CPU by Pipelining. (True/False)?

* True

1. We can increase the clock speed of a CPU by Pipelining. (True/False)?

* False

1. "Pipelining will always increases performance" do you agree? Explain?

* No, because of the pipeline hazards sometimes performance decreases.

1. What are the three types of hazards related to pipelining?
   1. **Structural Hazards:**

They arise from resource conflicts when the hardware cannot support all possible combinations of instructions in simultaneous overlapped execution.

* 1. **Data Hazards**:

They arise when an instruction depends on the result of a previous instruction in a way that is exposed by the overlapping of instructions in the pipeline.

* 1. **Control Hazards**:

They arise from the pipelining of branches and other instructions that change the PC.

1. Consider the following information about a CPU architecture:

* Number of pipeline stages =5
* Clock cycles needed to perform each pipeline stage=3
* If a program has 50 instructions without any branch or loops, calculate the number of

Clock cycles required to execute the program?

E = c (k + (n-1))

= 3 (5 + (50-1))

=3 x 54 = 162 clock cycles.

**Q 04**

1. If I = number of instructions in a program, CPl = average cycles per instruction And T = clock cycle time,
2. Define CPU Execution Time in terms of I, CPI and T

Execution Time = I\*CPI\*T

Consider the data given below:

Clock Rate = 3 GHz

Average Cycles per Instruction = 3

Number of instructions in a program = 310

1. Calculate clock cycle time?

* T=

1. Calculate the CPU execution time of this program?

= 310 \* 3 \*

1. Briefly explain "Seek Time", "Rotational latency (delay)" and Access time of hard disk drive operation.

* The seek time measures the time it takes the head assembly on the actuator arm to travel to the track of the disk where the data will be read or written.
* Rotational latency (sometimes called rotational delay or just latency) is the delay waiting for the rotation of the disk to bring the required disk sector under the read-write head.
* The access time or response time of a rotating drive is a measure of the time it takes before the drive can actually transfer data.

1. Consider the following details of a Hard Disk

* Average seek time = 6ms.
* Disk rotation speed = 7600 rpm
* 512 bytes/ sector
* 300 sectors/track (on average)
* 20,000 tracks/ surface
* Disk has 3 platters

1. Calculate the average rotational latency

* Tavg rotational latency = 1/ 2 × 1/ rpm × 60 Sec/ 1 min

= 1/ 2 × 1/ 7600 × 60 × 1000

= 3.95 ms

1. Calculate the capacity of this hard disk

* Disk capacity = 512 bytes/ sector × 300 sectors/ track × 20000 track/ surface × 2 surface/ platter × 3 platters/ disk

= 18,432,000,000 bytes

= 18.432 GB

1. Calculate the total time needed to read 150KB data file (assume the file is not fragmented)

* Tavg transfer = 1/ rpm × 1/ ( avg #sector/ track) × 60 Secs/ 1 min

= 1/ 7600 × 1/ 300 × 60000

= 38 ms

* 1 sector transfer time = 38 ms
* Transfer time of 150 KB = 38/ 512 × 150 × 1024

= 11400 ms

* Total time = avg seek time + avg rotational latency + transfer time

= 6 ms + 3.95 ms + 38 ms

= 47.95 ms

**Q 05**

1. Why process scheduling is important?

* Be fair, be efficient, Maximize throughput, Minimize response time, Maximize resource use etc.

1. What is the difference between preemptive and non-preemptive scheduling?

* **Non-Preemptive:** Non-preemptive algorithms are designed so that once a process enters the running state (is allowed a process), it is not removed from the processor until it has completed its service time.
* **Preemptive:** is the act of temporarily interrupting a task being carried out by a computer system, without requiring its cooperation, and with the intention of resuming the task at a later time.

1. Describe FCFS and Round Robin scheduling algorithms?

* **FCFS:** With this algorithm, processes are assigned the CPU in the order they request it.
* **Round Robin scheduling:** time slices are assigned to each process in equal portions and in circular order, handling all processes without priority.

1. Using preemptive shortest job first algorithm, indicate the order of execution of each process in a time line and calculate the average waiting time for the processes given below.

|  |  |  |
| --- | --- | --- |
| Process | Arrival Time (in sec) | Service Time (in sec) |
| P1 | 0 | 7 |
| P2 | 2 | 4 |
| P3 | 4 | 1 |
| P4 | 5 | 4 |
| P5 | 15 | 6 |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Idle Time |  |  |  |  |  |
|  |  |  |  |  |  |

|  |  |  |  |
| --- | --- | --- | --- |
| Process | Arrival Time (in sec) | Service Time (in sec) | Waiting time |
| P1 | 0 | 7 |  |
| P2 | 2 | 4 |  |
| P3 | 4 | 1 |  |
| P4 | 5 | 4 |  |
| P5 | 15 | 6 |  |

Average waiting time =

1. What is mean by deadlock?

* A deadlock is a situation in which two or more competing actions are each waiting for the other to finish and thus neither ever does.

**2015**

**Q 01**

1. What is the difference between combinational circuit and sequential circuit?

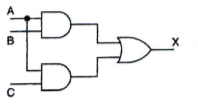
* Combinational circuit: the input values explicitly determine the output.
* Sequential circuit: the output is a function of the input values as well as the existing state of the circuit.

1. Which gates are called “Universal gates” and why?

* NAND gates
* NOR gates.

Because they can be used to implement other gates. It means every gate can be created by NAND and NOR gates only.

1. Consider the given logic circuit.



1. Draw the truth table for the circuit.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| A | B | C | AB | AC | X=AB+AC |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 |

1. Give an expression for above circuit using both Boolean variables and minters.

* X=AB+AC =>X=A (B+C)

1. Simplify the expression using K-map.

|  |  |  |  |
| --- | --- | --- | --- |
|  |  |  |  |
|  |  |  |  |

1. Consider the given truth table.

|  |  |  |
| --- | --- | --- |
| A | B | X |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

1. Give the Boolean expression

* X= AB’+A’B

1. Which basic logic gate present in the above table?

* XOR gates.

1. Implement a logic circuit for above table using minimum number of 2 input NAND gates. (Use Boolean algebra)

**Q 02**

1. Give the functions/ purpose of the following registers.
2. **IR (Instruction Register)**

* Contains the instructions most recently fetched.

1. **PC (Program Counter)**

* Contains the address of an instruction to be fetched.

1. **MAR (Memory Address Register)**

* Contains the address of location in memory.

1. **MBR/ MDR (Memory Buffer Register)**

* Contain a word of data to be written to the memory or the word most recently read.

1. What is meant by fetch and execute cycles in CPU operations?
2. **Fetch:**

* IR is examined
* If indirect addressing, indirect cycle is performed
* Rightmost n bits of MBR (address part of instruction) transferred to MAR
* Control unit requests memory read.
* Result (address of operand) moved to MBR.

1. **Execute:**

* May take many forms, depends on instruction being executed
* May include
  + Memory read/write
  + Input / Output
  + Register transfers
  + ALU operations

1. Explain 3 types of pipeline Hazards and state the solutions to avoid pipeline hazards.
2. Types:

* Structural Hazard
* Data Hazard
* Control Hazard

1. Consider a 7 phase pipelining architecture, explain how many clock cycles are needed to complete the execution of 8 instructions. (Assume 1 cycles for 1 phase)
2. Compare and contrast the RISC and CISC.

|  |  |
| --- | --- |
| CISC | RISC |
| Emphasis on hardware | Emphasis on software |
| Includes multi-clock complex instructions | Single-clock, reduced instruction only |
| Memory-to-memory: "LOAD" and "STORE" incorporated in instructions | Register to register: "LOAD" and "STORE" are independent instructions |
| Small code sizes, high cycles per second | Low cycles per second, large code sizes |
| Transistors used for storing complex instructions | Spends more transistors on memory registers |

**Q 03**

1. List two features for each Static RAM (SRAM) and Dynamic RAM (DRAM)?

* **Static RAM (SRAM)**
* Each cell stores bit with a six –transistor circuit.
* Faster and more expensive than DRAM.
* **Dynamic RAM (DRAM)**
* Each cell stores bit with a capacitor and transistor.
* Sensitive to disturbances.

1. Define the following with respect to Disk Access Time for a Hard Disk
2. **Seek Time (Tavg seek**)

* Time to positioning heads over cylinder containing target sector.
* Typical Tavg seek=9ms

1. **Rotational Time (Tavg rotation)**

* Time writing for first bit of target sector to pass under r/w head
* Tavg rotation=1/2\*1/RPMs\*60sec/1min

1. **Transfer Time(Tavg transfer)**

* Time to read the bits in the target sector.
* Tavg transfer=1/RPM\*1/(avg #sector/track)\*60sec/1min

1. **Average time to access some target sector (Taccess)**

* Taccess=Tavg seek+Tavg rotation+Tavg transfer

1. The features given below are of the hard disk

* Rotational rate=7200RPM
* Average seek time=9ms
* 512 bytes/sector
* 400sectors/track(on average)
* 20,000tracks/surface
* 2surfaces/platter
* 5platters/disk

Use the above features to calculate the following

1. Rotational latency(Tavg rotation)

= ((60/7200)\*1000\*1/2) ms

= 4.16ms

1. Transfer time(Tavg transfer)

= ((60/7200)\*1000\*1/400) ms

= 0.02ms

1. Average time to access some target sector(Taccess)

= 4.16ms+0.02ms+9ms

= 13.18ms

1. Capacity of hard disk in GB

= 512\*400\*20000\*2\*5

= 20.48GB

1. What is cache misses?

* Cache miss is a state where the data requested for processing by a component or application is not found in the cache memory.

1. List three types of cache misses?

* Cold(compulsory) miss
* Conflict miss
* Capacity miss

**Q 04**

1. List three buses that make up the system bus?

* Data bus
* Address bus
* Control bus

1. Give three reasons why an I/O device or peripheral device is not directly connected to the system bus?

* There are a wide variety of peripherals with various methods of operation. It would be impractical to include the necessary logic within the processor include the several devices.
* The data transfer rate of peripherals is often much slower than that of the memory or processor. Thus it is impractical to use the high speed system bus to communicate directly with a peripheral.
* Peripherals often use different data format and word length than the computer to which they are attached.

1. Explain three major functions of an I/O module?

* **CPU communication**
* I/O modules must communicate with the processor and with the external device.
* CPU communication involves the following:
* Command decoding:
* CPU commands are typically sent as signals on the control bus.
* Data:
* Exchanging between CPU and I/O modules over the data bus.
* Status reporting:
* Important to know the status of the I/O modules.
* Address Reconization:
* I/O module must recognize one unique address for each device it controls.
* **Device communication**
* I/O modules must be able to perform device communication.
* This involves commands, status and data.
* Data buffering
* Data coming from main memory are sent to an I/O module in a rapid burst.
* This data buffered in the I/O module and then send to the device at this rate.
* In the opposite direction, data are buffer so as not to tie up the memory in a slow transfer operation.

1. “The input /output operations can be performed by three basic techniques”
2. Name two of the above techniques?

* Programmed (polling)
* Interrupt driven

1. Describe why direct memory access (DMA) is considered an efficient mechanism for performing (I/O)?

* DIRECT ACCESS MEMORY: the device controller transfers an entire block of data directly to or from its own buffer storage to memory, with no intervention by the CPU
* With DMA, the system’s memory can be accessed without going through the CPU, allowing the hardware to access memory even if the CPU is busy. Thus, I/O devices can access memory in a shorter amount of time since they don’t have to wait for the CPU to free up.
* Only one interrupt is generated per block, to tell the device driver that the operation has completed, rather than the one interrupt per byte generated for low-speed devices.

1. Write two advantages of serial bus and two disadvantages of parallel bus?

* **Serial bus:**
* Less pins needed meaning more GPIO available for other stuff
* Requires faster speed to transfer the same image, meaning slower refresh rate.
* **Parallel bus:**
* More pins needed
* Faster refresh rate at same clock speed

**Q 05**

1. Explain the term of deadlock what are the reason to occur a deadlock?

* Dead lock:

A deadlock is a situation in which two computer programs sharing the same resource are effectively preventing each other from accessing the resource, resulting in both programs ceasing to function.

* Reasons:
* Mutual execution
* Hold and wait
* No preemption
* Circular wait

1. What are the solutions used for deadlocks?

* Prevention
* Avoidance
* Detection & recovery
* Do nothing

1. Let CPI is the average cycles per instruction use to measure the CPU performance. Consider the data given below.

* Clock rate=2.4GHz
* CPI=4
* Number of instructions in program=500

Calculate the CPU execution time of this program?

* CPU time= (instruction count\*CPI)/clock rate

= (500\*4)/2.4\*109 sec

= 0.83\*10-6 sec

1. Briefly explain about the CPU scheduling in multiprogramming operating system?

* Before multiprogramming was introduced the role of the operating system was simple and straight-forward-load a program in to memory and execute it via the CPU. Job scheduling refers to the selection of jobs to load into memory. CPU scheduling refers to the selection of a job existing in memory to execute via the CPU.

1. Suppose that the processes arrive in order: p1, p2, p3, p4 following shortest job first (SJF) method. Calculate the average waiting time with following details

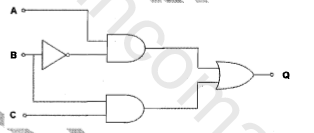
|  |  |
| --- | --- |
| process | Burst time |
| P1 | 6 |
| P2 | 8 |
| P3 | 7 |
| P4 | 3 |

Average wait time=

**2016**

**Q 01**

1. Consider the following logic gates



1. Draw the truth table for the circuit

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| A | B | B | C | A.B | B.C | Q |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 |

1. Give the Boolean expression for the about circuit

* Q= A.B+B.C

(ii). Simplify the following Boolean expression using algebra.

1. X=C.(A+C’)

X= C.A+C.C

C.A+0 (Complement law)

X= C.A

1. Y= A.C’+A.B.C’+A’C’D’+A’C’D

= A.C’ (1+B) +A’C’ (D’+D) (Complement law)

= A.C’.1+A’C’ (D’+D) (Annulment law)

= A.C’+A’C’.1 (Complement law)

= A.C’+A’C’

= C’ (A+A’)

= C’.1 (Complement law)

=C’

1. Z=AB+A’C+BC

= AB+A’C+BC (1) (Identity law)

= AB+A’C+BC (A+A’)

= AB+A’C+ (BC.A) + (BC.A’) (Distributive law)

= AB+A’C+A (BC) +A’ (CB) (Commutative law)

= AB+A’C+ (AB) C+ (A’C) B (Associative law)

= AB+ (AB) C+A’C+ (A’C) B (Commutative law)

= AB (1+C) + A’C(1+B) (Distributive law)

= AB.1+A’C.1 (Complement law)

= AB+A’C

(iii). Apply the de. Morgan’s theorem to simplify A+(B+C)

A+ (B+C)

= A. (B+C)

= A. (B+C)

= AB+AC

1. Simplify the following Boolean function F using k-map

F=AB’C+AB’C’+A’B’C’+A’B’C’

BC BC BC BC

|  |  |  |  |
| --- | --- | --- | --- |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 |

**Q 02**

1. Briefly explain the following:
2. **PC(Program Counter)**

* A special register, determines the location in memory (memory address) from which the next instruction will be fetched.

1. **MAR(Memory Address Register)**

* CPU register that either stores the memory address from which data will be fetched to the CPU or the address to which data will be sent and stored

1. **MBR(Memory Buffer Register)**

* Contains the data that was read or that is going to be written to the Memory.

1. **ALU(Arithmetic and Logical Unit)**

* An ALU is a digital circuit used to perform arithmetic and logical operations. It represents that fundamental building block of the central processing unit of a computer. Modern CPUs contain very powerful and complex ALUs

1. Briefly explain opcode and operand in a machine instruction

* An opcode means “operation code” .it is a single instruction that can be executed by the CPU. Opcode is a command such as MOV or ADD or JMP

E.g: MOV, AL, 34h

* According to the above example, the opcode is the MOV instruction the other parts are the called the “operands”. The operands are the register named AL and the value 34 hex

1. Explain instruction pipelining and mention at least 4 stages of pipelining?

* Instruction pipelining is a technique that implements a from of parallelism called instruction-level parallelism within a single processor.it therefor allows faster CPU throughput than would otherwise be possible at a given clock rate. The basic instruction cycle Is broken up into a series called a pipeline
* Fetch instruction
* Decode instruction
* Calculate instruction
* Executed instruction
* Fetch operands
* Write result

1. “Instruction pipelining increases the through put of CPU but some of the problems appear, which are reduce the through put of CPU during pipelining. Identify and analyses three problem which are decrease the performance of pipelining?

* **Pipeline Hazards** are situations that prevent the next instruction in the instruction stream from executing in its designated clock cycle Hazards reduce the performance from the ideal speedup gained by pipelining Three types of hazards

1. **Structural hazards:-**Arise from resource conflicts when the hardware can’t support all possible combinations of overlapping instructions
2. **Data hazards:-**Arise when an instruction depends on the results of a previous instruction in a way that is exposed by overlapping of instruction in pipeline
3. **Control hazards:-**Arise from the pipelining of branches and other instructions that change the PC (Program Counter

**Q 03**

1. Compare and contrast the static random access memory(SRAM) and dynamic random access memory(SRAM)
   * + **Static RAM (SRAM)**
     + Each cell stores bit with a six-transistor circuit.
     + Retains value indefinitely, as long as it is kept powered.
     + Relatively insensitive to disturbances such as electrical noise.
     + Faster and more expensive than DRAM**.**
     + **Dynamic RAM (DRAM)**

* Each cell stores bit with a capacitor and transistor.
* Value must be refreshed every 10-100 ms.
* Sensitive to disturbances.
* Slower and cheaper than SRAM.

1. Briefly explain “seek time” ,”rotational latency” and “transfer time” of a hard disk drive operation
   * + **Seek time** measure the time it takes the head assembly on the actuator arm to travel to the track of the disk where the data will be read or written.
     + **Rotational latency** is the delay waiting for the rotation of the disk to bring the required disk sector under the read write head.
     + **Transfer time** for a disk operation is the time require to transfer the data from (or to) the disk surface to (or from) the computer once the start of the data is under the R/W head.

* Transfer time based on

Speed of rotation

Density of data on the track

Amount of data to be transferred

1. Consider the following details of hard disk:

Average seek time = 6ms

Disk rotation speed = 7600 rpm

512 bytes /sector

400 sector /track (on average)

20 000 tracks / surface

Disk has 5 platters

1. Calculate the average rotational latency?

= 1/2\*60/7600sec

= 228,000 sec

1. Calculate the capacity of this hard disk?

= (byte)\*(sectors/track)\*(track)\*(surface)\*platters

= 512\*400\*20 000\*2\*5

= 40,960, 000,000 byte

= 38.14 GB

1. Calculate the total time needed to read 300KB data file

t avg transfer time = 60000/7600 \*1/400

= 0.019ms

512 byte = 0.019ms

300 KB = 0.019/512\*300\*1024

=11.4 ms

Access time = avg seek time + avg rotational time+ transfer time

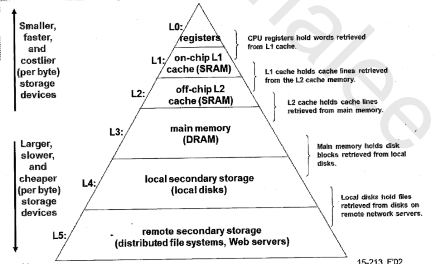
= 6 + 3.94 + 11.4

= 21.34 ms

1. Explain function of cache memory?

* Cache memory, lies in between CPU and the main memory.it also called CPU memory that a computer microprocessor can access more quickly than it can access regular RAM. The main function of cache memory is to speed up the working mechanism of computer.

1. Using memory hierarchy diagram ,explain each type of memory in the hierarchy and their characteristic?



**Q 04**

1. Write down the three type of buses in the CPU system and briefly explain?

* Data bus
* Address bus
* Control bus
* **Data bus**

A bus which carries a word or a data to or from memory is known as data

Bus. Data lines are bidirectional. One part of the data bus runs between RAM and

The Micro Processor. Another part of the data bus runs between RAM and various

Storage device

* **Address bus**

The address bus carries memory address it is unidirectional, the bits flow in

Only one direction

* **Control bus**

The control bus carries the control signals between the units of computer

The signals like READ/WRITE, START/HALT, etc. are carried by a control bus

1. State down any four major function of an input /output module?
   * + Control & timing
     + CPU communication
     + Device communication
     + Data buffering
     + Error detection
2. Briefly explain the following techniques in input output module?

* **Programmed I/O:**
* Data are exchanged between the CPU and I/O module.
* CPU executes a program and issue command directly to the appropriate I/O.

Ie: CPU has direct control over I/O:

* + - * Sensing status.
      * Read/write commands.
      * Transferring data.
* I/O module performs the requested action and set the appropriate bits in the I/O status register.
* No further action to alert the CPU.
* CPU waits for I/O module to complete operation.
* Periodically checks the I/O status register.
* This wastes CPU time.
* I/O Commands:
* To execute an I/O related instruction, CPU issues an address:
* Identifies module (& device if more devices).
* CPU issues an I/O command:
* Control - Telling module what to do.
  + - * Eg: Spin up disk.
* Test - Check status.
  + - * Eg: Power?, Error?
* Read:
  + - * Takes data from the device and places it in internal buffer.
* Write:
  + - * Takes data from the data bus and transmits to the device.
* **Interrupt driven I/O**
* With interrupt driven I/O:
* CPU:
* Issues an I/O command to a module.
* Continues to execute other instructions.
* I/O module:
* Interrupts the CPU when completed the work.
* Requests service to exchange data with the CPU.
* CPU then executes the data transfer.
* This:
* Overcomes CPU waiting.
* No repeated CPU checking of device
* I/O module:
* Receives a READ command from CPU.
* Proceeds to read data from the external device.
* Signals an interrupt to the CPU over control line:
* When the data are in the module’s data register.
* Waits until its data are requested by the CPU.
* Places its data on the data bus:
* When the CPU request is made.
* Ready for another I/O operation
* CPU:
* Issues a READ command.
* Goes off and does other work.
* Checks for interrupt at the end of each instruction cycle.
* If interrupted:
* Save the context (PC and CPU registers) of current program.
* Process the interrupt:
  + - * Reads the data from the I/O module and stores it in memory.
* Restores the saved context and resumes interrupted program execution.

* **Direct Memory Access (DMA)**
* Interrupt driven and programmed I/O require active CPU intervention:
* Every word of data from memory to I/O or from I/O to memory must pass through the CPU.
* Both I/O suffer from two inherent drawbacks:
* I/O transfer rate is limited by the speed with which CPU service a device.
* CPU is tied up in managing I/O transfers.
* The solution is DMA
* DMA Function:

(iv) External device are not generally connected directly into the computer bus structure” briefly explain this statement?

* Need i/o modules because of CPU speed is higher than other , different format of data transmission, transmit different amount of data, speed of device are different , increase the productivity of computer

1. Give the advantage of single bus “single bus , integrated DMA-I/O” over “single bus detached DMA”
   * DMA controller may support more than one device
   * May be a part of an i/o modules
   * May be separate module that controls one or more i/o s
   * Each transfer uses bus once

**Q 05**

1. Briefly explain why process scheduling is important?

* Be fair, be efficient, maximize throughput, minimize response time, maximize resource use etc.

1. Let CPI=average cycles per instruction ,I=number of instruction in a programmer and T=clock cycle time
2. Define CPU execution time in term of I ,T and CPI

Execution time =I\*CPI\*T

Clock rate=4GHz

Average cycles per instruction = 3

Number of instruction in a program = 400

1. Calculate clock cycle time?

* T=1/4\*10 sec

(C) Calculate CPU execution time of this program?

* 400\*3\*1/4\*10 sec

1. What is preemptive and non \_preemptive scheduling mean?

* Non preemptive scheduling: when a process enters the states of running, the state of that process is not detect from the scheduler until it finishes its services time preemptive scheduling: the preemptive scheduling is prioritized the highest priority process should always be the process that is currently utilized.

1. Using preemptive shortest job first algorithm, indicate the order of execution of each process in a time line and calculate the average waiting time for the processes given below?

|  |  |  |
| --- | --- | --- |
| Process | Arrival time(in sec) | Service time(in sec) |
| P1 | 8 | 3 |
| P2 | 2 | 1 |
| P3 | 1 | 3 |
| P4 | 3 | 2 |
| P5 | 4 | 4 |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Idle time | P3 | P2 | P4 | P5 | P1 |
| 0 1 | 4 | 5 | 7 | 11 | 14 |

|  |  |  |  |
| --- | --- | --- | --- |
| Process | Arrival time(in sec) | Service time(in sec) | Waiting time |
| P1 | 8 | 3 | 3 |
| P2 | 2 | 1 | 2 |
| P3 | 1 | 3 | 0 |
| P4 | 3 | 2 | 2 |
| P5 | 4 | 4 | 3 |

Average waiting time = (3+2+0+2+3)/5

= 10/5

= 2second

1. What is meant by deadlock?

* A deadlock is a situation in which two or more competing action are each

Waiting for the other to finish, and thus neither ever does.

**2017**

**Q 01**

1. A, B and C are inputs of following circuits.

A X

B

Z

C Y

(a) Write the Boolean expression of x, y and z?

* X= A+B’

Y= B.C

Z= (A+B’) + B.C

(b) Draw the truth table for the above circuit outputs of x, y and z?

|  |  |  |  |
| --- | --- | --- | --- |
| A | B | C | Z |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

1. Consider the following truth table

|  |  |  |
| --- | --- | --- |
| A | B | X |
| 0 | 1 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

Which is the logic gate initiated in the above truth table?

* NAND gate

1. Which type of circuit is output also consider as feedback (input)?

* In sequential circuit

1. Simplify the following Boolean expressions by Boolean algebra. Mention suitable laws for each step?
2. F=A.(A=B)

= A (Absorption)

1. F=AB+AB’+C

= A (B-B’)-C (Distributive Law)

= A.1-C (Inverse Law)

= A-C (Identity Law)

1. F=B+(AB)’

= B+ (A’+B’) (DE. Morgan’s Law)

= B+ (B’+A’) (Cumulative Law)

= (B+B’) +A’ (Associative Law)

= 1-A’ (Inverse Law)

= 1 (Null)

1. Simplify the following Boolean function F by K-Map

F=A’BC’ + AB’C + A’BC + A’B’C’

C/AB 01 11 10

0

|  |  |  |  |
| --- | --- | --- | --- |
| 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 |

1

F= A’B+ A’C+AB’C’

**Q 02**

1. List 03 main function of the CPU (Central Processing Unit)

* Fetch Instruction
* Interpret Instruction
* Fetch Data

1. Briefly explain 03 types of DMA (Direct Memory Access) configuration

* **Single-bus, detached DMA:**
  + Each transfer uses bus twice:
  + I/O to DMA then DMA to memory.
  + CPU is suspended twice.
  + Inexpensive but inefficient.
* **Single-bus, integrated DMA-I/O:**
* DMA controller may support more than one device.
* May be a part of an I/O module.
* May be separate module that controls one or more I/O
* Each transfer uses bus once:
* DMA to memory.
* CPU is suspended once.
* **I/O bus:**
  + Separate I/O Bus.
  + Bus supports all DMA enabled devices.
  + Each transfer uses bus once:
  + DMA to memory.
  + CPU is suspended once.

1. Briefly explain the following Registers
2. **MAR (Memory Address Register):-**

* Specific the address in memory of the data to be written from or read in to the MAR.

1. **IR (Instruction Register):-**

* Contains the 8-bit opcode instruction being executed.

1. **PC (Program Counter):-**

* Contains the address of the next instruction pair to be fetched from memory.

1. **MBR(Memory Buffer Register)**

* Contains data to be stored in memory or sent to the I/O unit, or is used to receive data from Memory or from the I/O unit.

1. In the design of computers, an instruction pipeline is a technique which is used to increase the instruction throughput of computer, pipeline consists of six stages
2. State 2 stage of pipeline

* Fetch instruction
* Decode instruction

1. Explain 3 types of pipeline hazards.
   1. **Structural hazards:-**Arise from resource conflicts when the hardware can’t support all possible combinations of overlapping instructions
   2. **Data hazards:-**Arise when an instruction depends on the results of a previous instruction in a way that is exposed by overlapping of instruction in pipeline
   3. **Control hazards:-**Arise from the pipelining of branches and other instructions that change the PC (Program Counter)

**Q 03**

* + 1. Capacity of a DVD-ROM is high and it is compared to a physically same size CD-ROM. What is the technology behind it?
* Bits are packed more closely on a DVD. The spacing between loops of a spiral (tracks) on a DVD is less compared to a CD. The DVD uses a laser with shorter wavelength. DVD also has layer technology.

* + 1. Define the terms “Seek time”, “Rotational delay”, and “Transfer rate” in hard disk operation.
* **Seek time: -** the time it takes for a disk arm to position itself over the required track.
* **Rotational time:** - is the delay waiting for the rotation of the disk to bring the required disk sector under the read-write head.
* **Transfer time: -** is the speed at which data is transferred to and from the disk media (actual disk platter) and is a function of the recording frequency.
  + 1. Suppose a hard disk drive has the following characteristic
* 4 patters
* 1024 tracks per surface
* 128 sectors per tracks
* 512 bytes per sector
* Average seek time = 5ms
* Disk rotational speed = 5000ms

1. What is the capacity of the hard disk?

= 4\*128\*1024\*512

= 268435456 bytes

= 256 Mb

1. Calculate the data transfer rate?

= 5000/60\*4\*128\*512

= 21845333 B/sec

= 20.83 Mb/sec

1. Calculate the rotational average latency?

= {(60/5000)\*1000}/2

= 6ms

* + 1. In computer architecture, the memory hierarchy separates computer storage into a hierarchy which is based on response time.
       1. What memory types has the fastest response as well as it is in top of the memory hierarchy?
* Registered
  + - 1. Compare and contrast SRAM and DRAM
* **Static RAM (SRAM)**
  + Each cell stores bit with a six-transistor circuit.
  + Retains value indefinitely, as long as it is kept powered.
  + Relatively insensitive to disturbances such as electrical noise.
  + Faster and more expensive than DRAM.
* **Dynamic RAM (DRAM)**
  + Each cell stores bit with a capacitor and transistor.
  + Value must be refreshed every 10-100 ms
  + Sensitive to disturbances.
  + Slower and cheaper than SRAM.

**Q 04**

1. List 03 major functions of I/O (Input/Output) module

* Control and timing
* CPU communication
* Device communication

ii. Describe the purpose of using “cache memory” and “virtual memory”

* **Cache memory** is a type of memory that lies between the CPU (Central Processing Unit) and the RAM (random Access Memory). The purpose of cache memory is to reduce the memory access time of the CPU from the RAM. The cache memory is much faster than Ram. So access time on cache is much lesser than the access time on RAM.
* **Virtual memory** is a memory management technique used in computers systems. The purpose of virtual memory is **to use the hard disk as an extension of RAM**, thus increasing the available address space a process can use.

iii. Compare and contrast CISC and RISC by using at least 4 features of hem.

**CISC RISC**

* Emphasis on hard work Emphasis on a software
* Includes multi-clock complex instruction Single clock, reduced instruction only.
* Memory-to-memory “LOAD” and “STORE” Registered to register. “LOAD” and

Incorporated in instruction “STORE” are Independent instruction.

* Small code sizes, high cycles per second low cycles per second, large code size
* Transistors used for storing complex Spend more transistors memory

Instruction. Registers.

iv.

1. Explain the term of “multiprogramming”

* In multiprogramming system there are one or more programs loaded in main memory which are ready to execute. Only one program at a time is able to get the CPU for executing its instruction (i.e., there is at most one process running on the system) while all the others are waiting their turn.

1. Calculate the average waiting time for the processes given below by using round robin algorithm.

|  |  |  |
| --- | --- | --- |
| process | Arrival time (in second) | Service time (in second) |
| P1 | 0 | 5 |
| P2 | 1 | 3 |
| P3 | 2 | 8 |
| P4 | 3 | 6 |

* Average wait time = (9+2+12+11)/4

= 8.5

**Q 05**

1. CPU scheduling decisions may take place under the four circumstances. State 3 of them.

* When a process switches from the running state to the waiting state (for I/O requests or invocation of wait for the termination of one of the child processes).
* When a process switches from the running state to the ready state (for example, when an interrupt occurs)
* When a process switches from the waiting state to the ready state (for example, completion of I/O)
* When a process terminates.

ii. Consider the data given below regarding a CPU

* Clock cycle time = 1/(2.8\*109) sec/cycle
* Average cycle per instruction = 4
* Number of instruction in program = 400

What is the CPU execution time of this program?

* = 400 \* 4 \*1/2.8\*109

iii. There are many different criteria to check to considering the best scheduling algorithm in CPU scheduling. Briefly explain four of them.

* **Utilization –** The function of time a device is in use. (ratio of in-use time/ total observation time)
* **Throughput –** The number of job completion in a period of time. (jobs/ second)
* **Service Time –** The time required by a device to handle a request. (second)
* Queuing Time – Time on a queue waiting for service from the device. (second)
* **Residence Time** – The time spent by a request at a device ( Residence Time= Service Time+ Queuing Time)
* **Response Time –** Time used by a system to respond to a user job. (second)
* **Think Time –** The time spent by the user of an interactive system to figure out the next request. (second)

iv.

1. What is the meaning of deadlock in operating system?

* A deadlock is a situation in which two computer programs sharing the same resource are effectively preventing each other from accessing the resource, resulting in both programs ceasing function.

1. Explain 3 methods of handling deadlock?

* Allow the system to enter a deadlock state and then recover
* Ensure that the system will never enter a deadlock state. The system can use either a deadlock prevention or avoidance.
* Ignore the problem and pretend that deadlocks never occur in the systems; used by most operating systems, including UNIX (need to restart your computer if a deadlock occur).

**2018**

**Q 01**

1. **“**There are two types of circuit. one is the input values which explicitly determine the Output and the other one is the output which depends on the input values as well as the existing state of the circuit” state two general categories of circuit.

* Combinational circuit
* Sequential circuit
* consider the half adder to answer the following questions

1. create the truth table from the above half adder

input-A

HALF adder

carry out co

input-B sum-s

1. create the truth table from the above half adder

|  |  |  |  |
| --- | --- | --- | --- |
| A | B | S | carry |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 |

1. construct a circuit diagram with minimum number of gates

A s-sum

B

c-carry

1. Draw the circuit diagram for the following Boolean expression by only using NAND gates

F(A,B)=AB+AB’=(AB+AB) =AB.AB

A A.B

A.B.A.B

B

B.B A.B

**4.** Simplify the following Boolean expression using Boolean algebra and its identities.

a. F(A,B)=A’ B+AB’+(AB )’

=A’B +AB’+A’+B’ (Demorgans law)

=A’B+A’+AB’+B’

=A’(B+1)+B’(A+1) (Identity law)

=A’.1+B’.1 (inverse law)

=0

1. F(A,B,C)=A’ B+ABC’+ABC

=A’B+AB(C’+C) (complement law)

=A'B+AB.1 (identity law)

=A’B+AB (complement law)

=B(A’+A) (complement law)

=B.1 (Identity law)

=B (identity law)

**5**. Symplyfy the following

F (A,B,C)=A’B’C’+AB’C+A’BC’+AB’C’+ABC’ using K-map.

AB 00 01 11 10

|  |  |  |  |
| --- | --- | --- | --- |
| 1 | 1 | 1 | 1 |
|  |  |  | 1 |

C

0

1

F=A’+AB’

**Q 02**

1. Briefly explain ALU.

* The arithmetic logic unit (ALU) carries out the logic operations (such as comparisions) and arithmetic operations (such as add or multiply) required during the program execute

Generally an ALU has two data inputs and one data output. Operations performed a often affect bits in the status register bits are set to indicate actions such as whether an over follow has occurred The ALU knows which operations to perform because it is controlled signals from the control unit.

1. State 4 registers which are inside the CPU.

* Instruction register
* Memory buffer register
* Memory data register
* Memory address register

1. “The IAS operates by repetitively performing an instruction cycle, each instruction cycle consists of two sub cycles fetch cycle and execute cycle .. Fetch cycle involves with different registers”

Describe the fetch cycle and mention the registers involved in cycle.

* The fetch cycle in a microprocessor comprises of several time states during which the next instruction to be executed is copied from the memory location (whose address is in the program counter) to the instruction register.
* Memory buffer register : a two way register that holds data fetched from memory or data waiting to be stored in memory.
* Current instruction register : a temporary holding ground for the instruction that has just been fetched from memory.

1. What are the three types of pipelining hazards? briefly explain them.
2. Pipeline hazards- are situations that prevent the next instruction in the instruction stream from executing in its designated clock cycle.
3. Structural hazards -Arise from resource conflicts when thehardware cant support all possibic combinations over lapping instructions.
4. Data hazards-Arise when an instruction depends on the results of a previous instruction in a way that is that is exposed by over lapping of instruction in pipeline
5. To deal with branches and reduce the branch penalty in pipelining there are several ways. Briefly describe 4 of them.
6. Prefetch branch target
   * + Target of branch is prepetched in addition to instruction following branch.
     + keep target until branch is executed.
     + Used by IBM 366191.
7. Loop buffer
   * + very fast memory.
     + maintained by fetch stage of pipe line.
     + check buffer before teaching from memory.
     + very good for small coops or jumps
     + cf cache
8. branch prediction (1)

Predict never taken

* Assume that jump will not happen
* Always fetch next instruction
* vax will not prefetch after branch if a page fault would result.

predict always taken.

* assume that jump will happen.
* always fetch target instruction.

Branch prediction (2)

predict by opcode

* some instructions are more likely to result in a jump than others
* Taken not taken switch,
* Based on previous history
* good for loops.

Delayed branch-rearrange instructions

**Q 03**

1. Briefly explain the function of cache memory?

* The basic purpose of cache memory is to store program instructions that are frequently re-referenced by software during operation.

Fast access to these instructions increases the overall speed of the software program. The main function of cache memory is to speed up the working mechanism of computer

1. “programs tend to reuse data and instructions used recently , or recently referenced by them. Briefly describe two types of locality.
   1. Temporal locality: recently referenced items are likely to be referenced in the near future.
   2. Spatial locality: items with near by addresses tend to be referenced close together in time.
2. What is nonvolatile memory? Give three example.

* Nonvolatile memories retain value even if powered off

EX.

* ROM(Read Only Memory)
* Hard disk
* Floppy memory

1. Describe the terms seek time, rotational latency, and transfer time in hard disk operations.

* Seek time : time to position heads over cylinder containing target sector.
* Rotational latency : time waiting for first bit of target sector to pass under r/w head.
* Transfer time: time to read the bits in the target sector .

1. Answer the questions based on following details of a hard disk.

512 bytes per sector

300 sectors per track(on average)

20000tracks per surface

Disk has 4 platters

2surfaces on each platters

Disk rotation speed is 7600 rpm

Average seek time is 9ms

* 1. Calculate the capacity of the hard disk.
  2. Calculate the transfer time.
  3. Calculate the rotational latency.
  4. Calculate the access time.

1. 2\*4\*20000\*300\*512bytes
2. 7600/60\*4\*300\*512

=77824000 B/sec

1. sec
2. 9ms+3ms=12ms

**Q 04**

1. State two techniques for input output operations.

* Programmed
* interrupt

1. Give 4 major function of I/O module.

* Control & timing
* CPU communication
* Device communication
* Data buffering
* Error detection

1. Differentiate preemptive and non-preemptive scheduling in CPU scheduling.

* Preemptive: the preemptive scheduling prioritized. The highest priority process should always be the process that is currently utilized.
* Non –preemptive : when a process enters the state of running, the state of that process is not deleted from the scheduler until it finishes its service time

1. State 5 criteria that can be used for performance evaluation of a scheduling algorithm.

* UTILIZAZION: the fraction of time advice is in use.
* THROUGHPUT: the number of job completions in a period of time.
* SERVICE TIME: the time required by a device to handle a request
* QUEUEING TIME : time on a queue waiting for service from the device
* RESIDENCE TIME : the time spent by a request at a device

1. The following table shows the processes, arrival times and the service required time. These processes are handled under preemptive shortest job first algorithm with quantum time one second.

|  |  |  |
| --- | --- | --- |
| Process | Arrival time(seconds) | Service time(seconds) |
| P1 | 2 | 6 |
| P2 | 5 | 2 |
| P3 | 1 | 8 |
| P4 | 0 | 3 |
| P5 | 4 | 4 |

1. Draw gantt chart for the above process scheduling

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| P1 | P2 | P3 | P2 | P4 | P1 | P5 |

1. “waiting time is the time interval for which one has to wait after placing a request for a service and before the service actually occurs”, calculate the waiting time of each process

|  |  |  |  |
| --- | --- | --- | --- |
| Process | Arrival time(seconds) | Service time(seconds) | Waiting time |
| P1 | 2 | 6 |  |
| P2 | 5 | 2 |  |
| P3 | 1 | 8 |  |
| P4 | 0 | 3 |  |
| P5 | 4 | 4 |  |

1. calculate the average waiting time

((2-2)+(6-5)+(8-1)+(16-0)+(19-4))/5

=39.5

=7.8

**Q 05**

1. Define clock rate(R) by using clock cycle time (T).

* The clock rate typically refers to the frequency at which the clock generator of a processor can generate pulses, which are used to synchronize the operations of its components, and is used as an indicator of the processors speed.it is measured in clock cycles per second or its equivalent, the SI unit hertz.

1. Find the CPU execution time of the following program
   1. Number of instructions in program (I)=300
   2. Average cycles per instructions (CPI) =3
   3. Clock rate =4GHz

=300\*3\* 1 sec

3\*109

=2.25\*10-7

1. Define the term, **‘deadlock’** using an example.

* A deadlock is a situation in which two or more competing actions are each waiting for the other to finish, and thus neither ever does.

1. Briefly describe three general strategies to handle deadlock.

* Allow the system to enter a deadlock state and they recover.
* Ensure that the system will never enter a deadlock state. The system can use either a deadlock prevention or avoidance.
* Ignore the problem and pretend that deadlocks never occur in the system;sed by most operating system, including UNIX

1. Computing systems are classified into four major categories in **flynn’s Taxonomy** briefly describe them.